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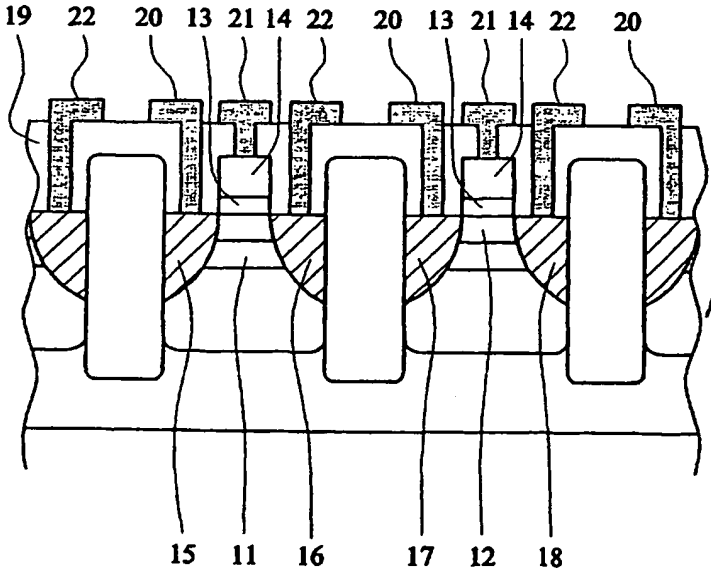
(54) Title: METHOD OF ISOLATING ADJACENT COMPONENTS OF A SEMICONDUCTOR DEVICE



(57) Abstract: A method of isolating adjacent transistors in CMOS devices having strained silicon (12) and silicon germanium alloy (11) layers is disclosed. A semiconductor device combines in a single CMOS device the advantages of surface n-channel strained silicon MOSFETs with those of buried p-channel compressively strained silicon-germanium MOSFETs, without the need to compromise the performance of either type of transistor. By forming electrically insulating barrier regions (8) before formation of the strained silicon layer (12), this avoids the problem of high temperature processing steps causing germanium to diffuse from layer (11) into the channels of transistors in layer (12) and thereby degrading the performance of the n-channel transistors formed by the method.

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METHOD OF ISOLATING ADJACENT COMPONENTS OF A SEMICONDUCTOR DEVICE

The present invention relates to a method of isolating adjacent components of a semiconductor device, and relates particularly, but not exclusively, to isolating adjacent transistors in CMOS devices having strained silicon and silicon germanium alloy layers.

NMOS transistors are known in which a silicon layer is grown on a layer of silicon-germanium alloy such that the silicon layer is under tensile strain. The separation of atoms in pure silicon is less than in pure germanium, and when the silicon layer is grown on the silicon-germanium alloy layer, the separation of the silicon atoms therefore increases to follow the atomic arrangement of the underlying silicon-germanium layer. The resulting silicon layer is under tension, and the tensile strain of the silicon layer improves the conductivity of electrons in the strained silicon. This phenomenon can be used to improve the speed of operation of NMOS transistors when the conduction channel is formed in the strained silicon layer.

PMOS devices are also known in which a silicon-germanium alloy layer with a higher density of germanium is grown on a silicon-germanium alloy layer having a lower germanium density. In a manner similar to the formation of a strained silicon layer, the atoms of the silicon-germanium layer of higher germanium density are arranged closer together, as a result of which that silicon-germanium layer is placed under compressive strain. This increases the conductivity of the layer to holes, which improves the speed of operation of PMOS transistors of which the hole conduction channels are formed in the silicon-germanium layer.

In CMOS type devices, which are the commonest type of microelectronic device, it is necessary to have both NMOS and PMOS transistors on the same device. However, when an attempt is made to integrate the NMOS and PMOS transistors of the above type in a single device, a problem arises when neighbouring transistors of the device are to be electrically isolated from each other. Conventional techniques for fabricating MOSFET isolation involve high temperature processing and several treatments such as etches and cleans. The etches and cleans remove silicon from the surface of the strained silicon layer. Whilst this is generally not a problem for MOSFETS not having strained silicon layers, the strained silicon layer of the NMOS device discussed above must be thinner than a predetermined critical thickness, or the layer forms defects in order to relax, and the improved electron conductivity of the layer is lost. However, conventional isolation processes remove too much silicon from the strained silicon layer, as a result of which if the strained silicon layer is thin enough to remain under tensile strain, the isolation process leaves insufficient silicon in the layer to form an adequate MOSFET conduction channel. In addition, the high temperature processing involved in conventional isolation techniques causes undesirable diffusion of germanium from the silicon-germanium layer through the strained silicon layer. This results in the presence of germanium in the channels of the devices, which degrades their performance.

WO02/13262 proposes a solution to the problem of excessive silicon removal during the etching and cleaning steps by providing an unstrained silicon-germanium layer on top of the strained silicon layer, the silicon-germanium layer acting as a sacrificial layer. However, the arrangement of WO02/13262 still suffers from the drawback of undesirable germanium diffusion caused by high temperature processing. As a result, the isolation of MOSFETs having strained silicon layers must be

carried out as a low temperature process, involving non-standard processing techniques. This greatly degrades the performance of such devices. The excess germanium in the conducting channel reduces the conductivity through alloy scattering and gate oxides grown on the surface do not incorporate germanium, leading to a snowploughing effect, which builds up additional germanium at the gate oxide interface.

Preferred embodiments of the present invention seek to overcome the above disadvantages of the prior art.

According to the present invention, there is provided a method of forming a semiconductor device, the method comprising the steps of:-

forming a substrate layer of a first semiconductor material;

forming a plurality of electrically insulating barrier regions such that the or each said barrier region extends into said substrate layer; and

forming a first conduction layer of a second semiconductor material, different from said first semiconductor material, on a first side of said substrate layer subsequently to formation of said electrically insulating barrier regions.

By forming said conduction layer subsequently to formation of said electrically insulating barrier regions, this provides the simultaneous advantages that the etching and cleaning steps used in forming the insulating barrier regions do not remove excessive material from the conduction layer, which is particularly important in the case where the conduction layer is formed from strained silicon. Also, the electrical isolation between adjacent transistors subsequently formed in the device can be formed using conventional high temperature processing,

while avoiding diffusion of material from adjacent layers into the conduction layer. For example, in case of a conduction layer of strained silicon being formed on a silicon-germanium layer, this minimises the diffusion of germanium into the n-channels of the strained silicon layer. This therefore provides the advantage that conventional manufacturing techniques can be used to fabricate the electrical isolation between adjacent transistors.

The first semiconductor material may have a lattice constant larger than that of pure silicon.

The conduction layer may be a first conduction layer of silicon under tensile strain.

The method may further comprise the step of forming a second conduction layer of silicon-germanium alloy between said first conduction layer and said substrate layer, said first conduction layer having a lattice constant in an unstrained state larger than that of said substrate layer, such that said first conduction layer is under compressive strain.

In a preferred embodiment, said second conduction layer is formed subsequently to formation of said electrically insulating barrier regions.

This provides the advantage that n-type or p-type wells, for surrounding source and drain regions of opposite polarity of transistors to be formed in the device, can be formed without the need to implant the wells through the first or second conduction layer, which minimises susceptibility of the device to damage. The therefore reduces undesirable doping of the first and second conduction layers, which could degrade conductivity of those layers.

The method may further comprise the step of forming wells of doped semiconductor material in said substrate layer, for surrounding respective source and drain regions of opposite polarity to the or each well of transistors to be formed in the device.

The method may further comprise the step of forming respective source and drain regions of a plurality of first field effect transistors in said first conduction layer, such that adjacent transistors of a plurality of pairs of adjacent said first transistors are electrically insulated from each other by a respective said electrically insulating barrier region.

The method may further comprise the step of forming respective source and drain regions of a plurality of second field effect transistors in said second conduction layer, such that adjacent transistors of a plurality of pairs of adjacent said second transistors are electrically insulated from each other by a respective said electrically insulating barrier region.

The method may further comprise the step of forming respective gate regions of a plurality of said first and second transistors on a side of said second conduction layer remote from said substrate layer, wherein each said gate region comprise a respective electrically conductive gate electrode and a respective electrically insulating layer between said gate electrode and the second conduction layer.
A preferred embodiment of the invention will now be described, by way of example only and not in any limitative sense, with reference to the accompanying drawings, in which:-

Figures 1 to 6 are schematic cross-sectional views showing steps in the formation of a semiconductor device embodying the present invention.

Referring to Figure 1, a CMOS heterojunction semiconductor device is formed by growing a virtual substrate 1 of silicon-germanium alloy on a silicon substrate 2, the silicon substrate 2 being in a relaxed state and the silicon-germanium alloy of the virtual substrate 1 having the formula $Si_{1-x}Ge_x$, where x varies between 0 and 0.25 and is typically 0.15. The wafer is then cleaned, and alignment marks for lithography steps defined on the wafer. A thin oxide layer 3 is then grown and a nitride layer 4 deposited on the oxide layer 3. In order to electrically isolate adjacent transistors to be formed in the device from each other, the nitride layer 4 is covered with photoresist 5 which remains after lithography in regions other than where electrical insulation is to be formed, and the nitride layer 4 and oxide layer 3 are etched away in the regions not covered by photoresist, to provide the arrangement shown in Figure 1.

As shown in Figure 2, a series of trenches 6 are formed by reactive ion etching in the regions not covered by photoresist, the trenches 6 extending downwards into the virtual substrate 1. An oxide liner 7 is then grown in the trenches 6, the oxide liner 7 forming a continuous layer with the oxide layer 3. Subsequently to formation of the oxide liner 7, the trenches 6 are filled with oxide filler 8. The device is then subjected to chemical mechanical polishing (CMP) and etching to provide the arrangement shown in Figure 2.

The arrangement of Figure 2 is then subjected to etching to remove the nitride layer 4, and p-type 9 and n-type 10 wells are formed in the virtual substrate 1 by ion implantation to provide the arrangement shown in Figure 3. As will be familiar to persons skilled in the art, the wells 9, 10 are to surround source and drain regions of opposite polarity semiconductor of transistors to be subsequently formed in the device. The oxide layer 3 is then removed by etching, and the p-type 9 and n-type

10 wells are electrically isolated from each other by insulating barrier regions formed by oxide fillers 8.

Subsequently to formation of the wells 9, 10, a first conduction layer 11 of silicon-germanium alloy having the formula $Si_{1-y}Ge_y$ where y is less than x+0.3 is then grown on the relaxed silicon-germanium substrate 1. Because of the higher average germanium density in layer 11 compared with virtual substrate 1, the separation of atoms in layer 11 is less than in virtual substrate 1, as a result of which layer 11 is under compressive strain. As will be familiar to persons skilled in the art, this significantly increases the conductivity of the layer 11 to holes compared with a relaxed layer (i.e. not under compressive strain) of the same material.

A second conduction layer 12 of silicon is then grown on silicon-germanium alloy layer 11. Because the separation of silicon atoms is less than in silicon-germanium, the silicon layer 12 is placed under tensile stress, which significantly increases the conductivity of layer 12 to electrons. Gate stacks, each of which comprises a gate oxide layer 13 and a polysilicon gate electrode 14 are then formed by growing a continuous layer of gate oxide 13, depositing a continuous layer of polysilicon 14, and using lithographic techniques and etching to define the gate region and then remove unwanted oxide and polysilicon. This arrangement is shown in Figure 4.

Referring now to Figure 5, source 15 and drain 16 regions of an n-channel transistor are formed by ion implantation and annealing, the source and drain regions extending downwards into the virtual substrate 1. Similarly, source 17 and drain 18 regions of a p-channel transistor are formed. At the end of this process, a continuous dielectric layer 19 of BPSG (boron phosphorous silica glass) is deposited over the top surface of the wafer as shown in Figure 5.

Finally, referring to Figure 6, contact windows are opened in dielectric layer 19 by lithography and etching, and metal for forming contacts to the gates, sources and drains of the transistors is deposited. The metal is then patterned using lithography and etched to leave source 20, gate 21 and drain 22 contacts respectively.

The device of Figure 6 combines in a single CMOS device the advantages of surface n-channel strained silicon MOSFETs with those of buried p-channel compressively strained silicon-germanium MOSFETs, without the need to compromise the performance of either type of transistor. Furthermore, by forming the electrically insulating barrier regions 8 before formation of the strained silicon layer 12, this avoids the problem of high temperature processing steps causing germanium to diffuse from layer 11 into the channels of transistors in layer 12 and thereby degrading the performance of the n-channel transistors.

It will be appreciated by persons skilled in the art that the above embodiment has been described by way of example only, and not in any limitative sense, and that various alterations and modifications are possible without departure from the scope of protection as defined by the appended claims. For example, instead of forming the silicon-germanium layer 11 directly on virtual substrate 1, an intermediate layer may be interposed between layer 11 and virtual substrate 1. Similarly, instead of forming tensilely strained silicon layer 12 directly on layer 11, an intermediate layer may be interposed between layers 11 and 12.

CLAIMS

1. A method of forming a semiconductor device, the method comprising the steps of:-

forming a substrate layer of a first semiconductor material;

forming a plurality of electrically insulating barrier regions such that the or each said barrier region extends into said substrate layer; and

forming a first conduction layer of a second semiconductor material, different from said first semiconductor material, on a first side of said substrate layer subsequently to formation of said electrically insulating barrier regions.

2. A method according to claim 1, wherein said first semiconductor material has a lattice constant larger than that of pure silicon.

3. A method according to claim 2, wherein said conduction layer is a first conduction layer of silicon under tensile strain.

4. a method according to claim 2 or 3, further comprising the step of forming a second conduction layer of silicon-germanium alloy between said first conduction layer and said substrate layer, said first conduction layer having a lattice constant in an unstrained state larger than that of said substrate layer, such that said first conduction layer is under compressive strain.

5. A method according to claim 4, wherein said second conduction layer is formed subsequently to formation of said electrically insulating barrier regions.

6. A method according to any one of the preceding claims, further comprising the step of forming wells of doped semiconductor material in said substrate layer, for surrounding respective source and drain regions of opposite polarity to the or each well of transistors to be formed in the device.

7. A method according to any one of the preceding claims, further comprising the step of forming respective source and drain regions of a plurality of first field effect transistors in said first conduction layer, such that adjacent transistors of a plurality of pairs of adjacent said first transistors are electrically insulated from each other by a respective said electrically insulating barrier region.

8. A method according to any one of the preceding claims, further comprising the step of forming respective source and drain regions of a plurality of second field effect transistors in said second conduction layer, such that adjacent transistors of a plurality of pairs of adjacent said second transistors are electrically insulated from each other by a respective said electrically insulating barrier region.

9. A method according to any one of the preceding claims, further comprising the step of forming respective gate regions of a plurality of said first and second transistors on a side of said second conduction layer remote from said substrate layer, wherein each said gate region comprise a respective electrically conductive gate electrode and a respective electrically insulating layer between said gate electrode and the second conduction layer.

10. A method of forming a semiconductor device, the method substantially as hereinbefore described with reference to the accompanying drawings.

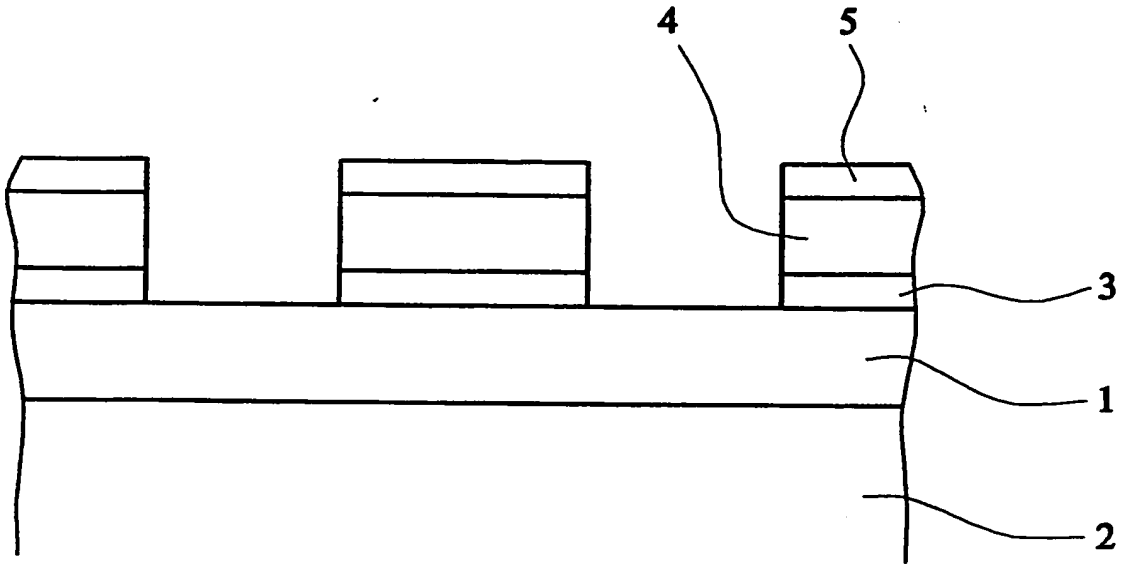

FIG. 1

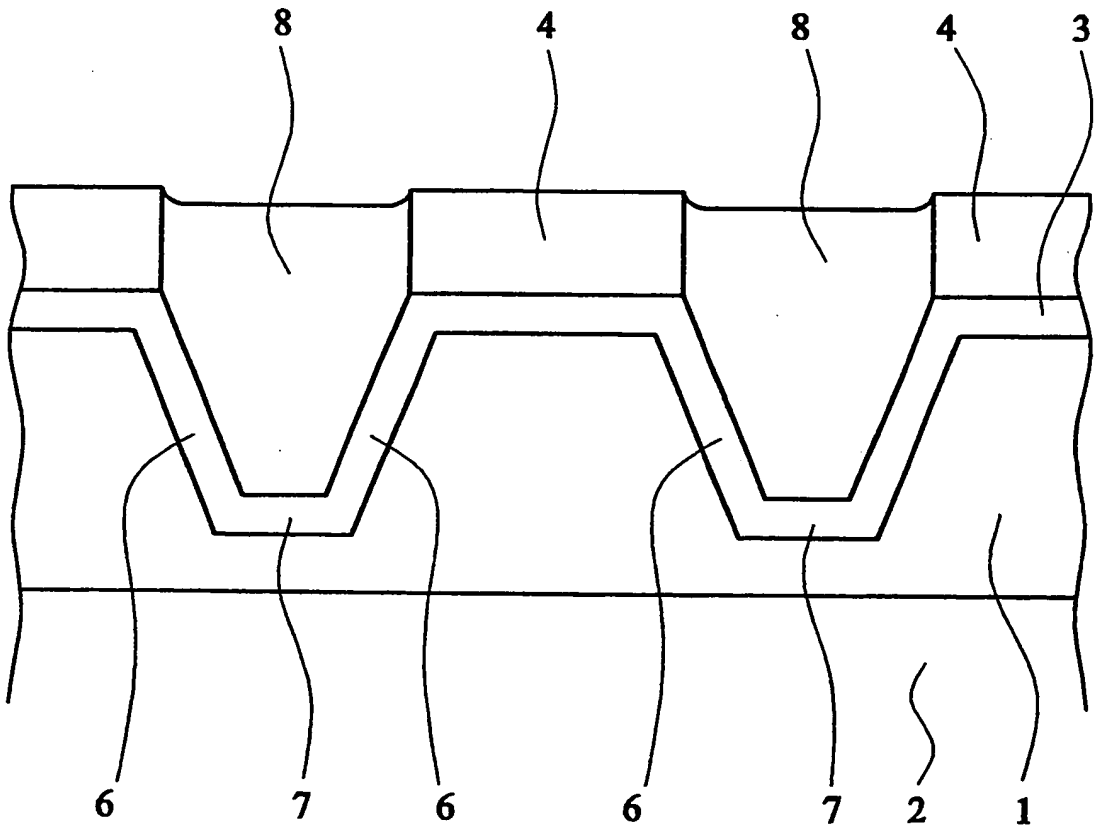

FIG. 2

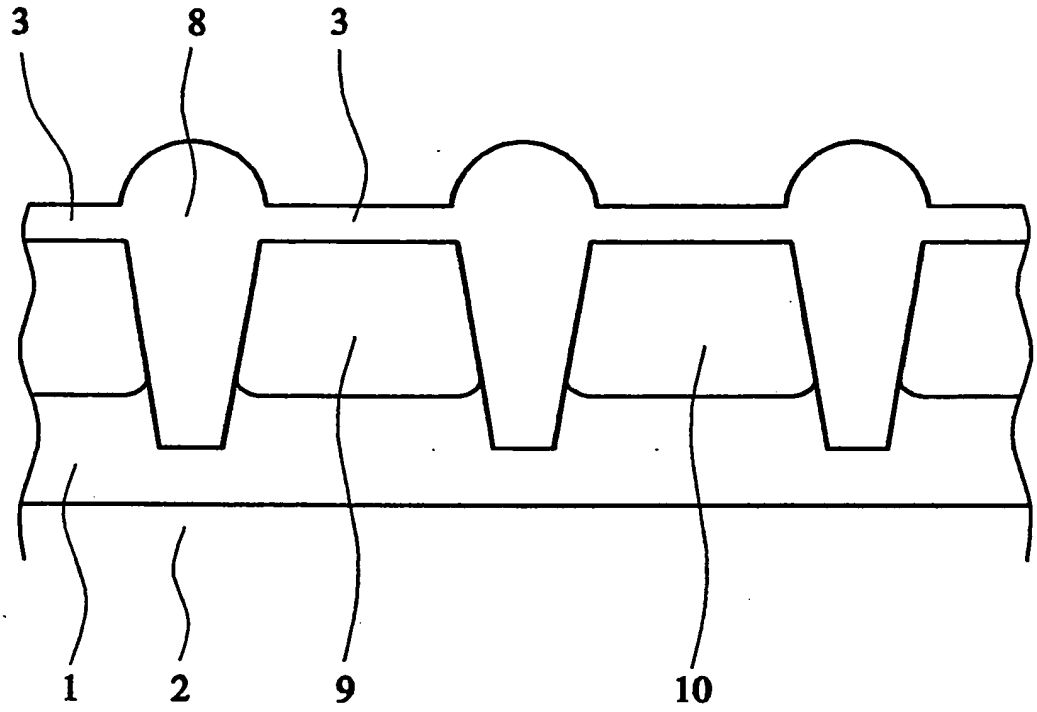

FIG. 3

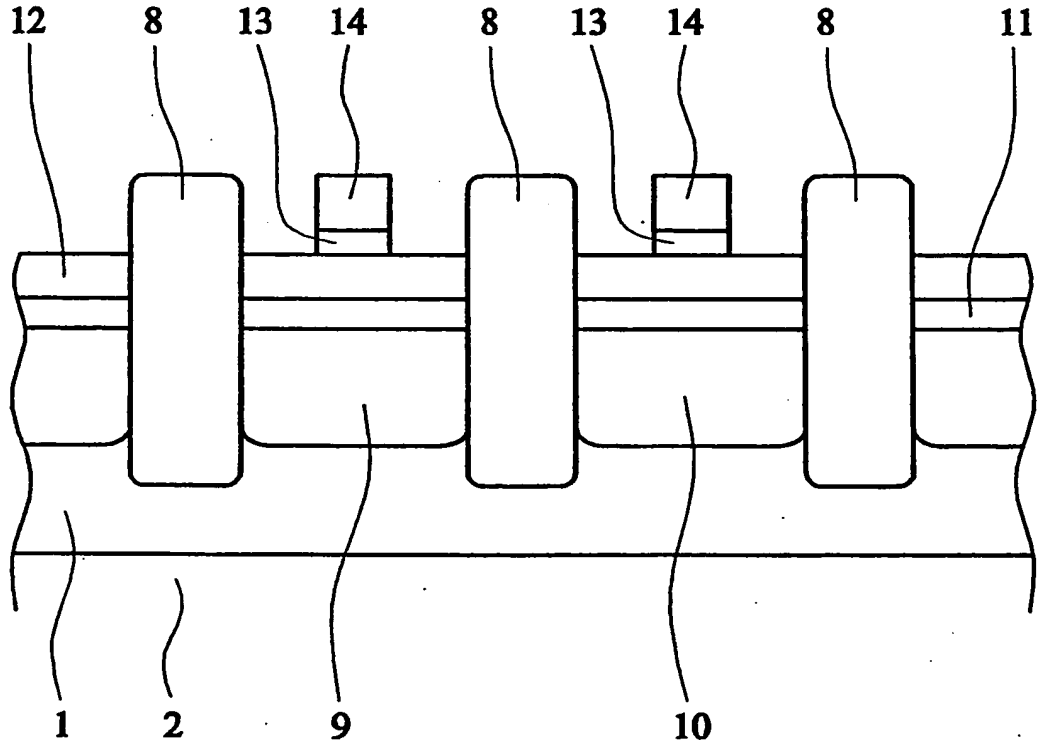

FIG. 4

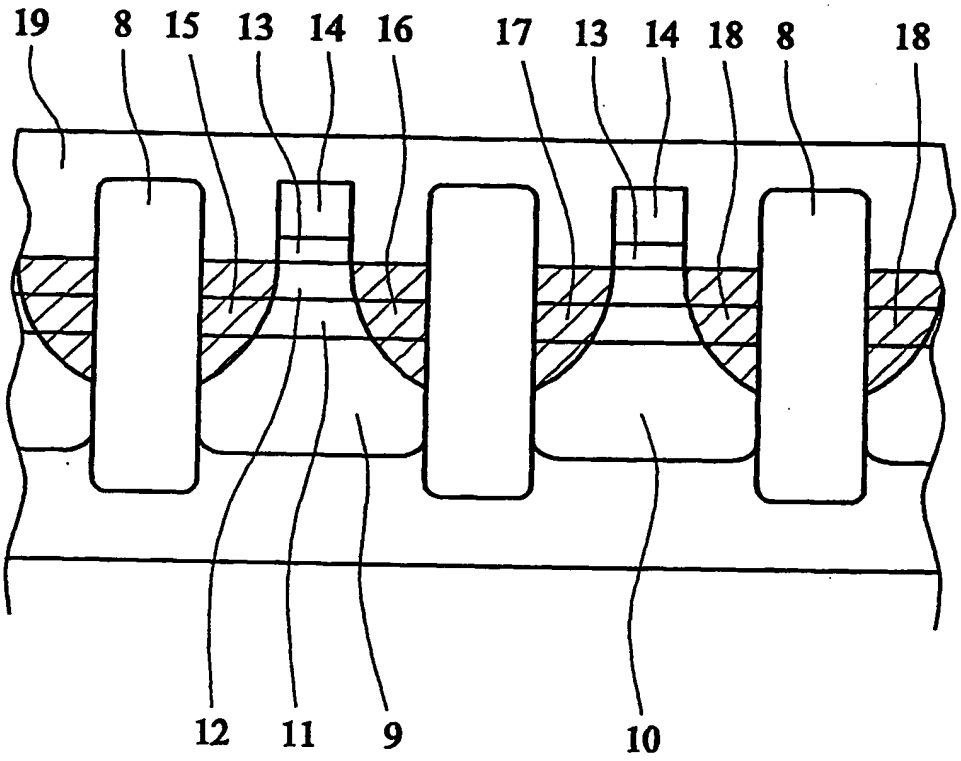
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FIG. 5

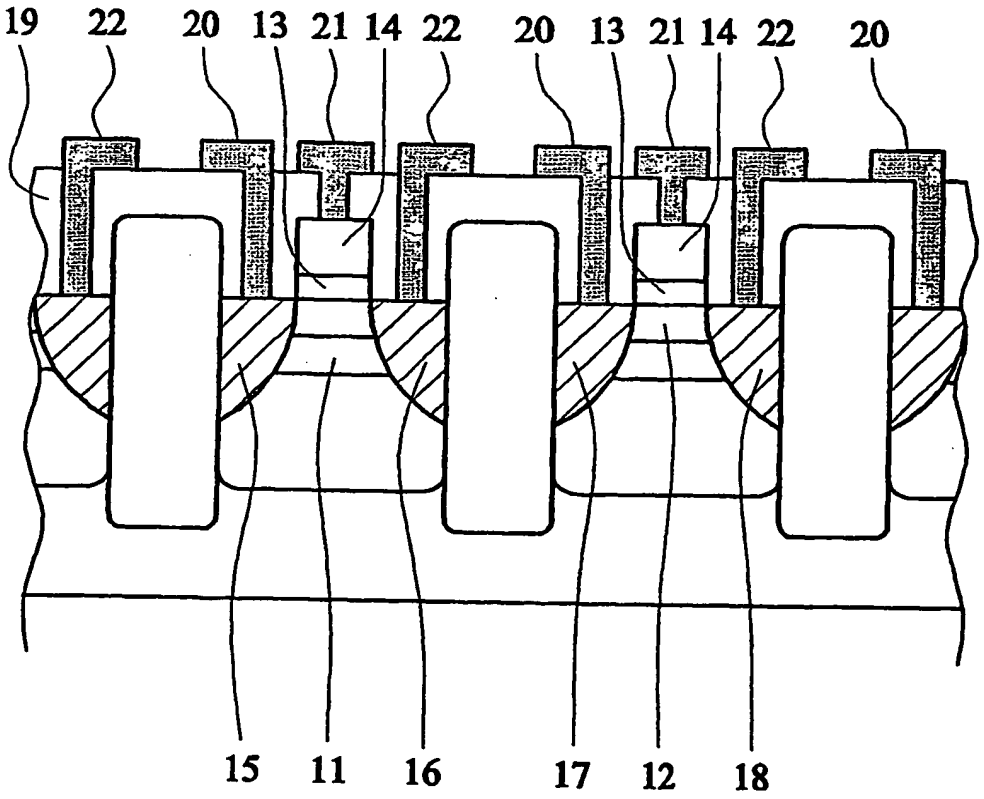
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FIG. 6